REMARKS

After entry of this amendment, claims 1-24 remain pending. In the present Office Action, claims 1-8 and 11-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by Pontius et al., U.S. Patent No. 6,029,243 ("Pontius"). Claims 9-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pontius in view of allegedly well known features. Applicants respectfully traverse these rejections.

Applicants respectfully submit that claims 1-24 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "a scheduler coupled to the register file and configured to schedule the floating point operation for execution, wherein the scheduler is configured to transmit one or more register addresses of operands of the floating point operation to the register file responsive to scheduling the floating point operation for execution, and wherein the prediction circuit is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution."

Pontius does not teach or suggest the above highlighted features. The Office Action asserts that the scheduler recited in claim 1 is the control device that uses the LAD and LAE information to determine the mechanism for executing the floating point instruction, either execution in hardware or trap (See Office Action, page 3, second full paragraph). However, the trap logic TPL, and more specifically the LAD and LAE circuits, detect the trap based on the operands read from the register bank. The operands read from the register bank are also provided directly to the execution unit EXU for execution (see Fig. 1, INA and INB). Thus, it is very clear that the operation of the TPL unit to detect the trap in the LAE occur after the operands have been read. Accordingly, the operation of the trap logic TPL cannot teach or suggest a prediction circuit that is configured to predict the execution latency prior to the floating point operation being scheduled by the scheduler for execution, where operands are read from the register file responsive to the scheduling the floating point operation.

Rather, Pontius teaches "logic for determining when to execute a floating point operation in hardware and when to trap makes its determination as a function of a requested result precision and the maximum apparent precision of the operands" (Pontius, col. 2, lines 30-34).

For at least the above-stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-15, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-15 recites additional combinations of features not taught or suggested in the cited art.

Claim 16 recites a combination of features including: "scheduling the floating point operation from a scheduler for execution in a floating point unit, wherein scheduling the floating point operation comprises transmitting one or more register addresses of operands of the floating point operation to a register file to read one or more operands of the floating point operation, and wherein the predicting is performed prior to the scheduling." The same teachings highlighted above with regard to claim 1 are alleged to teach the combination of features of claim 16. Applicants respectfully submit that the cited art does not teach or suggest the above highlighted features of claim 16, either. Accordingly, Applicants respectfully submit that claim 16 is patentable over the cited art. Claims 17-24, being dependent from claim 16, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 17-24 recites additional combinations of features not taught or suggested in the cited art.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91300/LJM.

Respectfully submitted,

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